AF/Final

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

DONALD C. ABBOTT ET AL.

Serial No. 10/724,498 (TI-28098.1)

Filed December 1, 2003

For: SEMICONDUCTOR CIRCUIT ASSEMBLY HAVING PLATED LEADFRAME INCLUDING GOLD SELECTIVELY COVERING AREAS TO BE SOLDERED

Art Unit 28114

Examiner Deilinh P. Nguyen

Customer No. 23494

CERTIFICATE OF MAILING OR TRANSMISSION UNDER 37 CFR 1.8

I hereby certify that the attached document is being deposited with the United States Postal Service with sufficient postage for First Class Mail in an envelope addressed to Director of the United States Patent and Trademark Office, P.O. Box 1450,, Alexandria, VA 22313-1450 or is being facsimile transmitted on the date indicated below:

5-12-06

Jay M. Cantor, Reg. No. 19,906

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

BRIEF ON APPEAL

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and/or interferences.

STATUS OF CLAIMS

This is an appeal of claims 17 to 22, all of the rejected claims. Claims 1 to 16 have been canceled. Please charge any costs to Deposit Account No. 20-0668.

STATUS OF AMENDMENTS

A response was filed after final rejection and entered for purposes of appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

In prior art fabrication of copper leadframes, the entire surfaces of the leadframe are plated with gold. This practice severely inhibits the adhesion of the leadframe segments to molding compounds and risks delamination in thermomechnical stress testing. Furthermore, the plating of the complete leadframe with a thin gold layer makes it impossible to decide by visual inspection whether a leadframe has the gold surface or not. Such standard simple inspection, however, is highly desirable as manufacturing practice. Finally, the deposition of gold in unnecessary areas is counterproductive to cost saving efforts.

An urgent need has therefore arisen for a low-cost, reliable mass production method for a leadframe having reduced palladium layer thickness combined with solderablility, bondability, adhesion capability to molding compounds, and visual inspection contrasts. The leadframe and its method of fabrication should be flexible enough to be applied for different semiconductor product families and a wide spectrum of design and assembly variations, and should achieve improvements toward the goals of improved process yields and device reliability. Preferably, these innovations should be accomplished using the installed equipment base so that no investment in new manufacturing machines is needed.

The above is accomplished, as set forth in claim 17 by providing a copper leadframe (301) having a mount pad (302) for an integrated circuit chip (303) and a plurality of lead segments (305) having their first end near said mount pad (305a) and their second end remote from said mount pad (305b). According to the method, the leadframe (101) is cleaned in alkaline soak cleaning and alkaline electro cleaning (page 10, line 15ff) and the leadframe is activated by immersing the leadframe into an acid solution, thereby dissolving any copper oxide (page 10, line 19ff). The leadframe is then immersed into an electrolytic nickel plating solution to deposit a first layer of nickel onto the copper (page 10, line 27ff) and a layer comprising an alloy of nickel and palladium is electroplated (page 10, line 28ff). A second layer of nickel is electroplated, thereby adapting said lead segments for mechanical bending (page 11, line 3ff). Then a layer of palladium is electroplated (page 11, line 13ff) and the chip pad and the first segment ends are selectively masked, thereby leaving the second segment ends exposed and a layer of gold is plated on the exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction between the gold-plated and unplated leadframe areas.

The above is accomplished as set forth in claim 22, the steps include providing a copper leadframe (301) having a mount pad (302) for an integrated circuit chip (303) and a plurality of lead segments (305) having their first end near the mount pad (305a) and their second end relatively remote from the mount pad (305b). According to the method, the leadframe is cleaned in alkaline soak cleaning and alkaline electro cleaning (page 10, line 15ff), the leadframe is activated by immersing the leadframe into an acid solution to dissolve any copper oxide (page 10, line 19ff) and a layer of nickel is electroplated to adapt the lead segments for mechanical bending (page 11, line 3ff). A layer of palladium is electroplated (page 11, line 13ff) and the

chip pad and the first segment ends are selectively masked to leave the second segment ends exposed. A layer of gold is plated on the exposed segment ends in a thickness suitable to optimize solder attachment to create a visual distinction between the gold-plated and unplated leadframe areas.

GROUNDS OF REJECTION

Claims 17 to 21 were rejected under 35 U.S.C.103(a) as being unpatentable over Akino et al. (J.P. No. 2000-77593) in view of Huang et al. (U.S. 5,994,767) and further in view of Grunwald et al. (U.S. 3,819,497).

Claim 22 was rejected under 35 U.S.C. 103(a) as being unpatentable over Huang et al. in view of Grunwald et al.

ARGUMENT

Claims 17 to 21 were rejected under 35 U.S.C.103(a) as being unpatentable over Akino et al. (J.P. No. 2000-77593) in view of Huang et al. (U.S. 5,994,767) and further in view of Grunwald et al. (U.S. 3,819,497). The rejection is without merit.

To begin with, Akino et al. is not available as a reference because the publication date of this reference is subsequent to the effective filing date (the provisional application) of the subject application.

The examiner now states that the rejection can be supported by Huang et al. and Grunwald et al. without Akino et al. without any reasoning being provided why Akino et al. was initially cited and remains cited. This is, of course, not the rejection of record.

While the official rejection still includes Akino et al., it will be demonstrated why the rejection is improper even without Akino et al., though this would be a new ground of rejection

Claim 17 requires, among other steps, providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad. The examiner cites Huang et al. to show a copper leadframe and apparently for no other reason. However, it is noted that Huang does not show a copper leadframe, but rather, at best, a copper coated leadframe (column 2, lines 16ff). However, it is conceded that copper leadframes were in the prior art.

Claim 17 further requires the steps of cleaning the leadframe in alkaline soak cleaning and alkaline electro cleaning (not shown or discussed as shown in Grunwald et al) and activating the leadframe by immersing the leadframe into an acid solution, thereby dissolving any copper oxide which is shown by Grunwald et al.

Claim17 further requires the step of immersing the leadframe into an electrolytic nickel plating solution and depositing a first layer of nickel onto copper. Nowhere is such a step taught or suggested by Grunwald et al.

Claim 17 further requires the step of electroplating a layer comprising an alloy of nickel and palladium onto the prior step. Nowhere is such a step taught or suggested by Grunwald et al.

Claim 17 further requires the step of electroplating a second layer of nickel, thereby adapting said lead segments for mechanical bending;. Nowhere is such a step taught or suggested by Grunwald et al.

Claim 17 then requires the step of `electroplating a layer of palladium. Nowhere is such a step taught or suggested by Grunwald et al.

Claim 17 still further requires the step of selectively masking the chip pad and the first segment ends, thereby leaving the second segment ends exposed and plating a layer of gold on the exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating

a visual distinction between the gold-plated and unplated leadframe areas. Nowhere are such steps taught or suggested by Grunwald et al.

In addition, it is noted that Grunwald et al. does not relate to leadframes and is from a different art area. Accordingly, any combination with Huang et al. is not suggested by the references themselves, but rather from the subject disclosure.

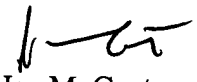
Claim 18 to 21 depend from claim 17 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 17.

Claim 22 requires, among other features, the step of providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near the mount pad and their second end relatively remote from the mount pad. The argument presented above for this step with reference to claim 17 is incorporated by reference as are the arguments for the steps of cleaning the leadframe in alkaline soak cleaning and alkaline electro cleaning, activating the leadframe by immersing said leadframe into an acid solution to dissolve any copper oxide, electroplating a layer of nickel to adapt the lead segments for mechanical bending, electroplating a layer of palladium, selectively masking the chip pad and the first segment ends to leave the second segment ends exposed and plating a layer of gold on the exposed segment ends in a thickness suitable to optimize solder attachment to create a visual distinction between the gold-plated and unplated leadframe areas.

CONCLUSIONS

For the reasons stated above, reversal of the final rejection and allowance of the claims on appeal is requested that justice be done in the premises.

Respectfully submitted,



Jay M. Cantor
Reg. No. 19906
(301) 424-0355
(972) 917-5293

CLAIMS APPENDIX

The claims on appeal read as follows:

17. A method for fabricating a leadframe comprising the steps of:

providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

cleaning said leadframe in alkaline soak cleaning and alkaline electro cleaning;

activating said leadframe by immersing said leadframe into an acid solution, thereby dissolving any copper oxide;

immersing said leadframe into an electrolytic nickel plating solution and depositing a first layer of nickel onto said copper;

electroplating a layer comprising an alloy of nickel and palladium;

electroplating a second layer of nickel, thereby adapting said lead segments for mechanical bending;

`electroplating a layer of palladium;

selectively masking said chip pad and said first segment ends, thereby leaving said second segment ends exposed; and

plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment, thereby creating a visual distinction between the gold-plated and unplated leadframe areas.

18. The method according to Claim 17 wherein said gold plating is performed electrolytically or electrolessly.

19. The method according to Claim 17 wherein said masked parts of said leadframe comprise the leadframe areas to be encapsulated by molding compound.

20. The method according to Claim 17 wherein the process steps are executed in sequence without time delays, yet including intermediate rinsing steps.

21. The method according to Claim 17 wherein said acid solution may be sulfuric acid, hydrochloric acid or any other acid.

22. A method for fabricating a leadframe comprising the steps of:

providing a copper leadframe having a mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end relatively remote from said mount pad;

cleaning said leadframe in alkaline soak cleaning and alkaline electro cleaning;

activating said leadframe by immersing said leadframe into an acid solution to dissolve any copper oxide;

electroplating a layer of nickel to adapt said lead segments for mechanical bending;

electroplating a layer of palladium;

selectively masking said chip pad and said first segment ends to leave said second segment ends exposed; and

plating a layer of gold on said exposed segment ends in a thickness suitable to optimize solder attachment to create a visual distinction between the gold-plated and unplated leadframe areas.

EVIDENCE APPENDIX

Not applicable

RELATED PROCEEDINGS APPENDIX

Not applicable